IN THE CLAIMS:

Please cancel claims 1-17 without prejudice.

Please add new claims 21-37.

--21. (New) An integrated circuit includes a gate structure disposed over a channel, a deep source region heavily doped with dopants of a first conductivity type, a deep drain region heavily doped with dopants of the first conductivity type, a source extension integral the deep source region, and a drain extension integral the deep drain region, wherein the drain extension is deeper than the source extension, wherein the integrated circuit is manufactured by a method, comprising:

providing the gate structure between a source location and a drain location in a semiconductor substrate;

providing an angled source extension implant in a direction from the source location to the drain location;

providing an angled drain extension implant in a direction from the drain location to the source location; and

providing a deep source/drain implant at the source location and the drain location.

22. (New) The integrated circuit of claim 21, further comprising providing a pair of spacers abutting lateral sides of the gate structure before the deep source drain implant.

23. (New) The integrated circuit of claim 22, wherein the providing the source extension step is a low energy, high dose ion implantation step.

24. (New) The integrated circuit of claim 23, wherein the drain extension implant step is a medium energy, high dose ion implantation step.

25. (New) The integrated circuit of claim 24, wherein a source extension formed by the source extension step is shallower than a drain extension formed by the drain extension implant step.

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26. (New) The integrated circuit of claim 25, wherein the source extension has approximately 5 times the concentration of dopants of the drain extension.

27. (New) The integrated circuit of claim 25, wherein the source extension has a concentration of $5x10^{19}$-$1x10^{20}$ of dopants per centimeter cubed and the drain extension has a concentration of $1x10^{19}$-$5x10^{19}$ dopants per centimeter cubed.

28. (New) The integrated circuit of claim 25, wherein the drain extension has a concentration between $1x10^{19}$ - $5x10^{19}$ dopants per centimeter cubed.

29. (New) The integrated circuit of claim 25, wherein the drain extension is more than 80 nm deep.

30. (New) The integrated circuit of claim 27, wherein the gate structure is associated with a N-channel or P-channel with MOSFET.

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31. (New) An ultra-large scale integrated circuit including a plurality of field effect transistors, the field effect transistors comprising:

a gate structure on a top surface of a semiconductor substrate;

a source extension with dopants of a first conductivity type;

a drain extension with dopants of the first conductivity type; and

forming deep source and drain regions with dopants of the first conductivity type, wherein the gate structure is between the source and drain regions, wherein the drain extension is deeper than the source extension.